CLAIMS

1. A method for developing fully functional transparent memory modules using chip parts, comprising the steps of:

testing the parts for failed segments;

sorting the parts according to the results of the testing;

identifying working segments in the parts; and

combining the working segments amongst different parts, including at least one partially defective parts, in an effective manner to create an effective fully functional transparent memory module.

2. A memory module made by the method of claim 1.

3. The method of claim 1, wherein at least one of the parts is a package.

4. The method of claim 1, wherein at least one of the parts must be replaced by a substitute part.

5. A memory module made by the method of claim 4, wherein the memory module is made up of repaired and the substituted parts.

6. The method of claim 1, wherein the combination of working segments is done by patching using solder-dot connections to provide a logical oring of sets of I/O lines on a printed circuit board.

7. The ~~process~~ method of claim 1, wherein the combination of working segments is done by patching using jumper installations on a printed circuit board.

8. A method for developing effective chip-on-board memory modules, using a combination of partially defective memory parts and good memory parts, comprising the steps of:

assembling the parts onto a chip-on-board module assembly;

testing the module for failed I/O lines in the parts;

identifying the operating segments in the parts, including at least one of the partially defective memory parts; and

combining the working segments in an effective manner to create an effective fully functional transparent memory module.

9. A chip-on-board memory module made by the method in claim 8.

10. The method of claim 8 further comprising the steps of:

pretesting the parts while in die form; and

sorting the parts according to the results of the pretesting.

11. A chip-on-board memory module made by the ~~process~~ method in claim 10.

12. A process for patching primary parts with partially defective memory parts to create a memory module functionally transparant to the user, comprising the steps of:

testing the primary parts and partially defective memory parts before mounting the parts on a board;

identify operating and failed segments of the primary parts and the partially defective memory parts;

determining which I/O lines from the partially defective memory parts to use for patching the failed segments of the primary parts; and

substituting I/O lines from the backup parts for failed lines in the failed segments of one or more primary components to form a resultant memory module.

13. A memory module made by the method of claim 12.

14. The method of claim 12 wherein the resultant memory module comprises all good and partially defective memory parts.

15. The method of claim 12, further comprising the step of replacing at least one of the parts with a replacement part.

16. A memory module made by the process of claim 15, wherein the memory module comprises all good, repaired and the replacement parts.

17. The method of claim 12, wherein the patching is done by using solder-dot connections to provide a logical oring of sets of I/O lines on a printed circuit board.

18. The method of claim 12, wherein the patching is done using jumper installations on a printed circuit board.

19. A ~~process~~ method for patching primary parts with partially defective parts, comprising the steps of:

perform a wafer test on memory die;

identify the working and nonworking segments in the parts;

package the primary and partially defective parts according to working segments;

test the parts;

give each part an identification code, the identification code containing a quadrant test pattern fo the part;

select parts for assembly on a module board;

assemble the parts on the module board according to the nature and location of the parts' working segments;

fill in the solder-dot locations of the primary parts, wherein the solder-dot locations of the back-up parts are left open;

test the module on a full function circuit tester, wherein failed bits are noted, and the module is assigned a new identification code designating the failed bits;

generate patching instruction charts for the module, wherein the development of the patching instruction charts includes an optimization pass designed to maximize use of smaller patch parts, leaving the larger parts availiable for patching later-discovered failures;

disconnect solder-dot connections on the primary parts to isolate the failed line;

fill the solder-dot connections to patch in the substitute lines, the solder-dot connections selected as identified in the patching instruction charts; and

re-test the module, including high temperature stress testing of the module.

20. The method of claim 19 wherein the disconnecting and filling steps are automated.

21. A memory module made by the method of claim 19.

22. The method of claim 19 wherein the resultant memory module comprises all good and partailly defective memory parts.

23. The method of claim 19, further comprising the step of replacing at least one of the parts with a replacement part.

24. A memory module made by the process of claim 19, wherein the memory module comprises all good, partially defective and the replacement parts.

25. A method for generating patching instruction traveler charts using optimization, comprising the following steps:

scanning bits of wider parts;

identifying unused bits in the smaller parts, wherein the unused bits will be used for substitution;

optimizing the selection of the parts to use in patching;

generating patching instructions; and

implementing the generated patching instructions into a traveler chart.

26. The method of claim 25, wherein at least one computer is used to automate all of the steps.

27. A module made up of primary parts and partially defective backup parts, comprising:

at least one primary part, the primary part having at least one line failure;

a plurality of partially defective parts;

a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing any failing primary part I/O lines to be replaced by I/O substitute lines from the backup parts.

28. The module of claim 27, wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the substitute line having the equivalent function as the failing line so that the module is transparent to the user.

29. The module of claim 27 wherein the module comprises all good and partially defective memory parts.

30. The module of claim 27, wherein the module contains at least one replacement part.

Sub a7

31. A module made by the process of claim 27, wherein the module comprises all good, partially defective and the replacement parts.

32. The module of claim 27 wherein the selection of substitute lines are identified in patching instruction charts developed for the module, wherein the development of the patching instruction charts includes part optimization.

33. A SIMM module made up of primary parts and partially defective parts, comprising:

at least two primary parts, at least one of the primary parts having at least one line failure;

a plurality of partially defective parts;

a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing the failing primary part lines to be replaced by I/O substitute lines from the partially defective parts ~~parts~~;

wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling

the applicable solder-dot, the substitute line having the equivalent function as the failing line so that the module is transparent to the user.

34. The module of claim 33 wherein the selection of substitute lines are identified in patching instruction charts developed for the module, wherein the development of the patching instruction charts includes part optimization.

35. The module of claim 33 wherein the module comprises all good and partailly defective memory parts.

36. The module of claim 33, wherein the module contains at least one replacement part.

37. A module of claim 33, wherein the memory module comprises all good, partially defective and the replacement parts.

38. The module of claim 33, wherein the primary parts are 1MX16 parts.

39. The module of claim 38, wherein the partially defective parts are 1MX4 parts.

40. A memory module made up of primary parts and partially defective backup parts, comprising:

four primary parts, each of the primary parts having at least one line failure;

eight partially defective backup parts;

a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing the failing primary part lines to be replaced by I/O substitute lines from the backup parts;

wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the replacement line having the equivalent function as the failing line so that the module is transparent to the user.

41. The memory module of claim 40, wherein the memory module is a 2MX32 memory module, the four primary parts consist of 1MX16 packages, and the backup parts consist of eight 1MX4 packages.

42. The memory module of claim 40, wherein each line in a primary part can be patched by a line from either one of the eight partially defective backup parts.

43. The module of claim 40, wherein the selection of substitute lines are identified in patching instruction charts developed for the memory module, wherein the development of the patching instruction charts includes part optimization.

44. The module of claim 40 wherein the memory module comprises all good and partailly defective memory parts.

45. The module of claim 40, wherein the memory module contains at least one replacement part.

46. A module of claim 40, wherein the memory module comprises all good, partially defective and the replacement parts.

47. A chip-on-board module made up of primary parts and partially defective backup parts, comprising:

at least one primary part, the primary part having at least one line failure;

a plurality of partially defective parts;

a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing any failing primary part I/O lines to be replaced by I/O substitute lines from the backup parts;

wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the replacement line having the equivalent function as the failing line so that the chip-on-board module is transparent to the user.

48. The memory module of claim 47, wherein the four primary parts consist of 1MX16 parts, and the backup parts consist of eight 1MX4 parts.

49. The module of claim 47, wherein the selection of substitute lines are identified in patching instruction charts developed for the module, wherein the development of the patching instruction charts includes part optimization.

50. A process for selecting primary parts and partially defective parts on a chip-on-board module assembly, comprising the steps of:

performing a wafer test on a memory die;

selecting a combination of parts that have a reasonable probability of being patched successfully;

selecting parts for assembly on a PC module;

assembling the parts on the PC module;

applying a plastic overcoating to the assembled parts; and

test the module using a chip test applied at the module pins.

51. The process of claim 50, further comprising the steps of:

assigning a bar code to the module to identify failed bits;

fill in the solder-dot locations of the primary parts, the solder-dot locations of the back-up parts are left open;

test the module on a full function circuit tester, wherein failed bits are noted, and the module is assigned a bar-code identifying the failed bits;

generate patching instruction charts for the module, wherein the development of the patching instruction charts includes an optimization pass designed to maximize use of smaller patch parts, leaving the larger parts availiable for patching later-discovered failures;

disconnect solder-dot connections ont the primary parts to isolate the failed line;

fill the solder-dot connections to patch in the substitite lines, the solder-dot connections selected as identified in the patching instruction charts;

re-test the module, including high temperature stress testing of the module.

52. The method of claim 51 wherein the disconnecting and filling steps are automated.

Sub a9

53. A memory module made up of primary parts and partially defective backup parts, comprising:

at least four primary parts, the primary parts having at least one line failure, and the primary parts are layed out horizontally with a card edge;

at least four partially defective parts;

a module PC board containing a pattern of solder-dot connections, the solder-dot connections allowing any failing primary part I/O lines to be replaced by I/O substitute lines from the backup parts;

wherein the failing line is disconnected from the primary part by removing the solder of its solder dot connection and the substitute line is connected by filling the applicable solder-dot, the replacement line having the equivalent function as the failing line so that the module is transparent to the user.

54. The memory module of claim 53, wherein the four primary parts consist of 1MX16 parts, and the backup parts consists of 1MX4 memory parts.

55. The memory module of claim 53, wherein two primary parts and two back-up parts are located on the front side of the board and the other two primary parts and the other two back-up parts are located on the back side of the board.

Sub a10

56. The memory module of claim 53, wherein at least one of the primary parts is a extedned data out part that runs at about 60 nsec.

57. The memory module of claim 53, wherein at least one of the primary parts is a extended data out part that runs at about 70 nsec.

58. The memory module of claim 53, wherein at least one of the primary parts is a Fast Page part.

59. The memory module of claim 53, further comprising a variable voltage regulator, the variable voltage regulator connected to the module PC board.

60. The memory module of claim 53, further comprising a variable voltage regulator, the variable voltage regulator connected to the module PC board, wherein the variable voltage regulator works with the extended data out primary part by tieing output enable to ground.

61. The memory module of claim 53, further comprising a variable voltage regulator, the variable voltage regulator connected to the module PC board, wherein the variable voltage regulator works with the Fast Page primary part by tieing output enable to ground.

62. The module of claim 53 wherein the resultant memory module comprises all good and partially defective memory parts.

63. The module of claim 53, wherein the resultant memory module contains at least one replacement part.

64. A module of claim 53, wherein the memory module comprises all good, partially defective and the replacement parts.

65. Any method for testing of the die level to decide the packaging type and the mixture of parts to be used on a memory module for optimum utilization, comprising the steps of; test a wafer; identify the working and nonworking segments in the parts; optimize utilization of working segments using decision tables to decide optimum packaging or combination of devices on a module.